Preliminary Software Specification

N20MA-M42P-4-00E Series

Absolute Magnetic Encoder SPI 4-wire Option

1 General Specification of SPI 4-wire Serial Communication

Item	Specification	Note
Transmission type	Serial Peripheral Interface(SPI)	
Communication type	Single-ended	
Synchronization type	Synchronous	
Communication Baud rate	Up to 10.0Mbps	
Transmission Error Checking	6/16 bits CRC	6 bits CRC equation G(X) = $X^6 + X^1 + 1$ 16 bits CRC equation G(X) = $X^{16} + X^{15} + X^{12} + X^7 + X^6 + X^4 + X^3 + 1$

Table 1 **General Specification of Serial Communication**

2 General Format Definition of Transmission Frames between Host and Encoder

2.1 Overview of Communications

A one-to-one serial communication is established between the encoder (Client) and the Host (e.g. a servo driver). The communication are in a single-ended transmission format that complies with SPI electrical standard. The encoder will carry out specific operations based on the command requests made by the host.

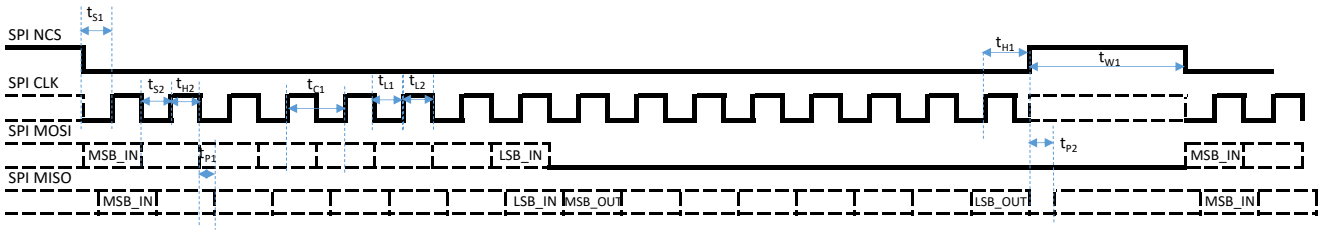

Figure 1 General transmission frames format for SPI-4Wires

NOTE

1. When NCS=1, MISO=high-Z. (to support Multi-Encoder Bus Mode)
2. During 1st 8 clocks, MISO always "echo" Operation Command received on MOSI (to support Multi-Encoder Mode)
3. SPI Mode 0 and SPI Mode 3

Symbol	Description	Min	Max	Unit
t_{C1}	Permissible Clock Cycle Time	100		ns
t_{L1}	Clock Signal low Level Duration	50		ns
t_{L2}	Clock Signal high Level Duration	50		ns
t_{S1}	Setup Time: NCS lo before SCLK low→high	50		ns
t_{H1}	Hold Time: NCS lo after SCLK low→high	80		ns
t_{W1}	Wait Time: between NCS low→high and NCS high→low	200		ns
t_{H2}	Hold Time: MOSI stable after SCLK low→high	15		ns
t_{S2}	Setup Time: MOSI stable before SCLK low→ high	15		ns
t_{P1}	Propagation Delay: MISO stable after SCLK high→low	35		ns
t_{P2}	Propagation Delay: MISO hi impedance after NCS low→high		35	ns

Table 2 **SPI 4-Wire Timing Specification**

2.2 Encoder Read Out Frame Sets Format and Timing

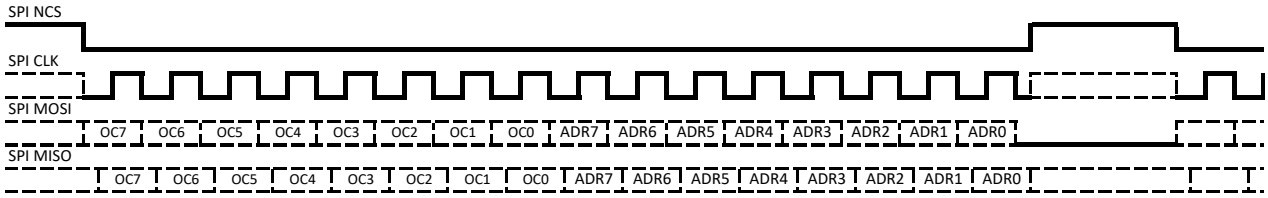

Figure 2 Register Read operation diagram

Operation Command (OC)	Description	Ports	CLK Bits															
			Byte1	Byte 2								Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
0xB0	Activate (1 encoder)	MOSI	B0	1	0	0	0	0	0	RA 0	PA 0								
		MISO	B0	0	0	1	0	0	0	0	0								
	Activate (2 encoder)	MOSI	B0	1	0	0	0	RA 0	PA 0	RA 1	PA 1								
		MISO	B0	0	0	0	0	1	0	0	0								
0xA6	Position Read	MOSI	A6																
		MISO	A6	Position Data + nError + nWarning + CRC/Position Data + nError + nWarning + nSequence + CRC														…	
0x81	Register Read (Continuous)	MOSI	81	ADDRESS(ADDR)								0x00							
		MISO	81	ADDRESS(ADDR)								0x00	DATA1	DATA2	…				
0xCF	Register Write (Continuous)	MOSI	CF	ADDRESS(ADDR)								DATA1	DATA2	…					
		MISO	CF	ADDRESS(ADDR)								DATA1	DATA2	…					
0x9C	Read Status	MOSI	9C																
		MISO	9C	0x00								ERR [7:0]	ERR [15:8]	ERR [23:16]	ERR [31:24]	WARN [7:0]	WARN [15:8]	WARN [23:16]	WARN [31:24]
0xD9	Write Command	MOSI	D9	COMMAND															
		MISO	D9	COMMAND															
0x97	Register Read (Single)	MOSI	97	ADDRESS(ADDR)															
		MISO	97	ADDRESS(ADDR)															
0xAD	Register Status/Data	MOSI	AD																
		MISO	AD	STATUS								DATA							
0xD2	Register Write (Single)	MOSI	D2	ADDRESS(ADDR)								DATA							
		MISO	D2	ADDRESS(ADDR)								DATA							

Table 3 **SPI 4-Wire Operation Commands**

2.2.1 Memory Read Command

Operation Command (OC) 0x81h [Continuous Read-on the current page of memory register] is used to read data from any register address in the ASIC chip. Refer to **Table 3** for the data streams sent on MOSI with OC 0x81h followed by the address of the first register to be read and a delay of 0x00. These three bytes will reflect on the MISO line before sending out the register address's (ADDR) data (DATA1). As long as the CLK continue to be sent, consecutive register address's (ADDR+1) data (DATA2) is transmitted and so forth. This procedure continued until the clocks end.

Operation Command (OC) 0x97h followed by 0xADh is used to perform Single read data from any register address in the ASIC chip.

2.2.2 Memory Write Command

Operation Command (OC) 0xCFh [Continuous Write-on the current page of internal memory register] is used to write data into any register address in the ASIC chip. Refer to **Table 3** for the data streams sent on MOSI with OC 0xCFh followed by the address of the first register to be written and the data. With each data byte the address of the register to be written is register address (ADDR+1). Data successfully received will be transmitted on MISO line.

Operation Command (OC) 0xD2h followed by 0xADh is used to perform single write data into any register address in the encoder memory and retrieve back the written data.

Note: Do not perform continuous write on external EEPROM

2.2.3 Memory Read Status Command (Single – STATUS Description)

Operation Command (OC) 0xAD STATUS (STAT) description as below:

Bit	Name	Description
7	Error/SC_EN	Invalid Operation Command/Specific Command enable
6:3	-	Reserved
2	Fail	Data request failed
1	Busy	Encoder busy
0	Valid	Data valid

Table 4 **Status bits description**

NOTE If the last OC received is 0xD9, STATUS bit-7 = 1 and the “Data” value reflects operation status.

2.2.4 SPI 4-Wire Specific Command

By sending an Operation Command (OC) 0xD9 followed by the Specific Code listed in the table below, the N20MA encoder performs the associated special task. Once the command is received by the encoder, perform 0xAD to read back the status of the operation. “Data” value if **0xFF** is error; if **0x00** is done; if “Code” is **in progress**. In case of overwritten operation example 0x97h register read, perform command operation 0x00(NOP) to put the operation status back to buffer for 0xAD.

Code	Name	Description
0x00	<NOP_OK>	<Return-code: last operation succeeded>
0x10	REBOOT	Reset, equivalent to power-cycle the encoder
0x18	MT_RESYNC	Re-synchronization of the MT device.
0x19	MT_RESET	Clear the FeRAM Value
0x20	SCLEAR	Clear the System Alarm and Warning registers
0x80	MTST_PRESET	Set current position as MT=0, ST=0
0x81	MT_PRESET	Set current position as MT=0
0xFF	<NOP_FAIL>	<Return-code: last operation failed>

Table 5 **Specific Command**

2.2.5 Error or Warning Readout and Descriptions

Operation Command (OC) 0x9C to perform error or warning bits readout. To perform segregation between Error or Warning bits please refer to Encoder Configuration Error and Alarm Setting.

Bits	Alarms	Alarms Definition
31:30, 27, 25:22, 18:17, 14:13, 10, 8:6, 3:0	Reserved	Default 0
28	MT Sync Error	To detect wrong MT Counting during MT Synchronization upon Startup Operation or MT Sync Retry Operation. 1 : Incorrect MT Sync 0 : MT Sync is correct
26	Multi-turn Err	To indicate bit jump occurs in Multi turn value. Compare MT delta for every 12.8us and the delta is > +/- 1 Rev. 1 : Bit Jump occurs 0 : No Bit Jump occurs
21	XC Error	To indicate MT Encoder Miss Count by comparing MT Encoder Counter Vs MT SW Counter. 1 : EHMT : Miss Count or XCERR value overflow. 1 : BBMT/Gear : Miss count 0 : No MT Miss count.
20	Speed MT Warning	To detect rotation speed >30kRPM for MT synchronization 1: Rotation speed exceeding the limit detected 0: No over speed detected
19	FeRAM CRC Error	To indicate multi-turn block FeRAM communication CRC Error. 1: Multi-turn FeRAM CRC error 0: No CRC error
16	FeRAM Register Error	To detect error on reading MT Hardware - FeRAM error 1: Error in FeRAM reading 0: No error in MT position reading
15	Chip Ready	To indicate the Encoder status. 1: Encoder is ready for normal operation (no fault status). 0: Encoder has abnormality due to other alarm bit(s) triggered.
12	TempErr	To indicate the temperature above the setting limit. 1 : Temperature above setting limit 0 : Temperature below setting limit
11	Memory Err	To indicate if loading of internal and external eeprom content upon encoder power up is successful. 1: Failure in loading internal EEPROM & external EEPROM memory data. 0: Loading external internal EEPROM & external EEPROM memory data successful.
9	STErr	To check the integrity of ST position. Mcode = absolute code. 1 : Mcode Jump or MLS-INC Miss Match or MLSErr flag. 0 : INC and Mcode function as normal.
5	Mag Hi	To detect error in the magnetic field sensing. 1: Magnetic field strength is too strong 0: Magnetic field strength is optimum for normal operation
4	Mag Lo	To detect error in the magnetic field sensing. 1: Magnetic field strength is too weak 0: Magnetic field strength is optimum for normal operation

Table 6 **Alarm or Error Bits Description**

2.2.6 Position Read

Operation Command (OC) 0xA6 is used to read absolute position data from the N20MA encoder. For nError (nE), nWarning (nW), CRC selections please refer to CRC setting in Table 13. Position latch is at the first rising clock. nError and nWarning trigger “0” if any of the error bits is triggered. Sequence Counter (Seq Cnt) is position read counter. Consecutive position read, the sequence counter (Seq Cnt +1) until 63 counts and then rollover become 0 and restart the counting. Single-turn bits (ST-bit) and Multi-turn bits (MT-bit) are a continuous bit that non-patch zero. Bits selection please refer to Table 18.

Operation Command(OC)	Description	Ports	1 byte	<MT-bit>	<ST-bit>	2 bits		6 bits	2 bytes
0xA6	Position Read	MOSI	A6(8b)						
	--> format = Basic	MISO	A6(8b)	MT Pos	ST Pos	nE	nW	CRC (6b)	
	--> format = Extended	MISO	A6(8b)	MT Pos	ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)

Table 7 **Multi-turn + Single-turn Position Read**

2.2.7 Enable Encoders

Operation Command (OC) 0xB0 is used to activate encoders in a bus mode connection. Register Data Access (RAx) is to access memory register in the encoder. Position Data Access (PAx) is to access position data in the encoder. “1” = Enable; “0” = Disable.

OC	Description	Ports	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0xB0	Activate (1 encoder)	MOSI	B0								1	0	0	0	0	0	RA0	PA0
		MISO	B0								0	0	1	0	0	0	0	0
	Activate (2 encoders)	MOSI	B0								1	0	0	0	RA0	PA0	RA1	PA1
		MISO	B0								0	0	0	0	1	0	0	0

Table 8 **Encoder Activation**

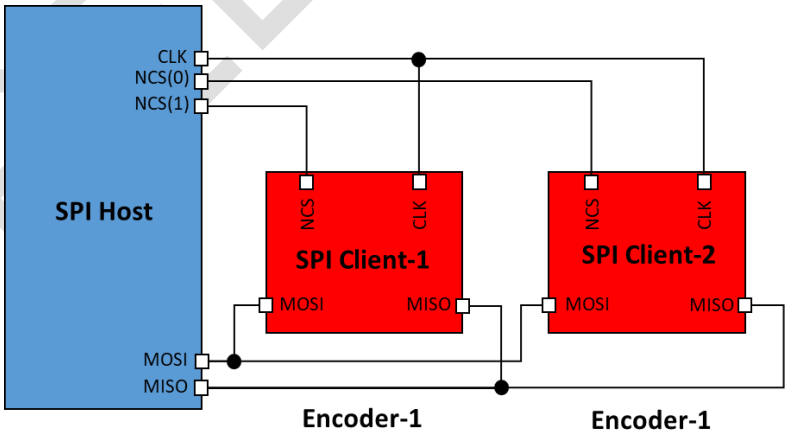

Figure 3 Bus Type connection for multi encoders

	Encoder 1								Encoder 2				
OC	**Description**	**Ports**	**1 byte**	**<Pos>**	**2 bits**		**6 bits**	**2 bytes**	**<Pos>**	**2 bits**		**6 bits**	**2 bytes**
0xA6	Position Read	MOSI	A6(8b)										
	--> format = Basic	MISO	A6(8b)	MT+ST Pos	nE	nW	CRC (6b)		MT+ST Pos	nE	nW	CRC (6b)	
	--> format = Extended	MISO	A6(8b)	MT+ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)	MT+ST Pos	nE	nW	Seq Cnt (6b)	CRC (16b)

Table 9 **Encoder Data output arrangement**

3 Encoder Memory Area

3.1 User Area

The N20MA supports 8kbits of register user area. The memory data are kept in a non-volatile memory. The available register pages that are accessible by the User.

Table 10 **User Memory Area with 8-kbit**

Page [decimal]	Address [hex]	Remarks
0 to 4	0x00~0x7E	User Area
11 to 13	0x00~0x7E	
Page Selection	0x7F	

NOTE

1. Total 8 pages with 127 addresses each are allocated for user access.
2. The active page numbers are specified in address 0x7F, page change is done by writing to address 0x7F. Default Page after power on is Page 0.
3. Once the page value is changed, allow a time delay of 18ms.
4. Typical EEPROM read time is 200µs minimum.
5. Typical EEPROM write time is 6ms minimum.

3.2 Encoder System Area

There are additional register pages reserved for system areas that are protected against accidental writing during operation. The memory data are kept in non-volatile memories.

Table 11 **Encoder System Memory Area**

Page [decimal]	Address [hex]	Remarks
5 ~ 8	0x00~0x7E	System Area
Page Selection	0x7F	

NOTE

1. Page 9 & 10 are volatile memory addresses reserved for encoder system use.

4 Encoder Configuration

4.1 Error and Warning Setting

To enable the Error or Warning in Operation Command (OC) 0x9C, set the respective bit to “1”, disable “0”

Page	Address [hex]	Bit								Initialize Value
		7	6	5	4	3	2	1	0	
7	28	SPI4W Warning Mask [31:24]								8'h00
	29	SPI4W Warning Mask [23:16]								8'h10
	2A	SPI4W Warning Mask [15:8]								8'h10
	2B	SPI4W Warning Mask [7:0]								8'h30
	2C	SPI4W Error Mask [31:24]								8'h14
	2D	SPI4W Error Mask [23:16]								8'h29
	2E	SPI4W Error Mask [15:8]								8'h0A
	2F	SPI4W Error Mask [7:0]								8'h00
	30	SPI4W Alarm Enable [31:24]								8'h14
	31	SPI4W Alarm Enable [23:16]								8'h39
	32	SPI4W Alarm Enable [15:8]								8'h1A
	33	SPI4W Alarm Enable [7:0]								8'h30
	34	SPI4W Alarm Latch Enable [31:24]								8'h14
	35	SPI4W Alarm Latch Enable [23:16]								8'h29
	36	SPI4W Alarm Latch Enable [15:8]								8'h0A
	37	SPI4W Alarm Latch Enable [7:0]								8'h00

Table 12 **Error and Warning bits configuration addresses**

4.2 Cyclic Redundancy Check Setting (CRC)

Page	Address [hex]	Bit								Default Value	Description
		7	6	5	4	3	2	1	0		
7	22				SPI4W_Ext_EN					8'h00	6bits CRC : “0” 16bits CRC : “1”
	26	SPI4W CRC [15:8]								8'h00	CRC Initial Value
	27	SPI4W CRC [7:0]								8'h00	

Table 13 **CRC settings**

4.3 Encoder Memory Map for Calibration and Special Functions

No.	Item	Address	Bits							
			7	6	5	4	3	2	1	0
1	Unlock Memory	0x00	Unlock Memory by Writing 0xAB							
2	Program Memory	0x01	Program Memory by Writing 0xC0							
3	Clear Alarm/Position	0x02						Alarm Clear	ST Zero Reset	MT Zero Reset
4	Calibration	0x04						OT_Direction-2	OT_Without_Accuracy	OT_Direction-1
5	Reset	0x0B	Perform Hard Reset by Writing 0xA7							
6	Alarm/Warning [31:24]	0x24	NA	NA	NA	MT Sync Error	NA	MT Error	NA	NA
7	Alarm/Warning [23:16]	0x25	NA	NA	XCErr	Speed MT Warning	FeRAM CRC Err	NA	NA	Feram ECC A/B Reg Err
8	Alarm/Warning [15: 8]	0x26	Chip Ready	Reserved	NA	Temp_Err	Memory Err	NA	ST_Err	NA
9	Alarm/Warning [7: 0]	0x27	NA	NA	Mag Hi	Mag Lo	NA	NA	NA	NA
10	Calibration Status	0x28	Mem_Busy	NA	Internal_Mem_Pass	Internal Mem_Fail	Zero_Done	Zero_Err	OT_Cal_Done	OT_Cal_Err

Table 14 **General Volatile Memory Map (Page 9, 0x09)**

NOTE

1. Memory Program Command is needed for the system area memory to be effective upon power cycle – applicable for changes to internal memory pages 5-8.
2. Perform Memory Program command for changes to any of the affected bank before moving to other non-volatile memory bank.
3. Changes will be lost after a power cycle without a Memory Program Command.

4.4 Counting Direction

Page [Decimal]	Address [hex]	Bit								Default Value
		7	6	5	4	3	2	1	0	
7	20	NA	Counting Direction	NA						8'h40

Table 15 **Register Bit for Counting Direction Selection**

With the default setting, position data is counting up when rotating in a counter-clockwise direction, as view from the top of the encoder.

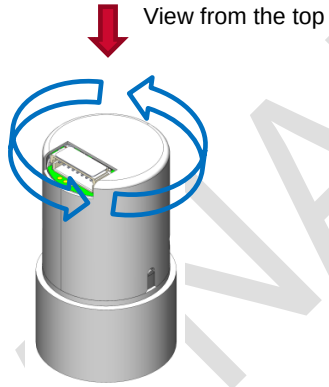

Figure 4 Default Counting direction

4.5 Zero Reset

The encoder zero reset data can be accessed by reading the addresses in Table 16.

Page	Address [hex]	Bit							
		7	6	5	4	3	2	1	0
7	0E	0	MT_ZR[38:32]						
	0F	MT_ZR[31:24]							
	10	MT_ZR[23:16]							
	11	MT_ZR[15:8]							
	12	MT_ZR[7:0]							
	13	ST_ZR[17:10]							
	14	ST_ZR[9:2]							
	15	ST_ZR[1:0]	6'b000000						

Table 16 **User zero-reset registers**

4.6 Multi-turn and Single-Turn Absolute Resolution Setting

Select the configuration for the absolute position output by updating the Page 7 Address 0x16, refer to Table 17 and Table 18.

Page	Address [Decimal]	Address [hex]	Bit								Default Value
			7	6	5	4	3	2	1	0	
7	22	16	NA	MT_Select[2:0]			NA	NA	ST_Select[1:0]		8'h53

Table 17 **Memory Map for Absolute Resolution Settings**

NOTE

1. Unlock Memory
2. Write in the new settings at Page 7, read back to ensure the setting is written successfully
3. Program Memory

MT_Select	
Bits	**Resolution**
000	0
001	12
010	14
011	16
100	20
101	**24**
110	32
111	39

ST_Select	
Bits	**Resolution**
00	15
01	16
10	17
11	**18**

Table 18 **Multi-turn and single-turn bits setting description**

4.7 Temperature Sensor

Read temperature value via register at Page 7 Address 0x05.

Temperature	TEMP[7:0]
-64℃	1100 0000
-40℃	1100 1110
-20℃	1110 1100
-1℃	1111 1111
0℃	0000 0000
1℃	0000 0001
10℃	0000 1010
25℃	0001 1001
50℃	0011 0010
85℃	0101 0101
127℃	0111 1111

Table 19 **Temperature Sensor Data**

NOTE

1. *Minimum support range for temperature output is -64 °C.
2. Negative values are from -1°C to -64°C only.
3. The maximum positive value is 191°C.

For the setting of temperature values and alarms, the configuration is as listed in Table 20 below. The temperature upper limit is defaulted to 0x7D, which is 125 °C, referenced to the ambient temperature as measured by the N20MA encoder ASIC.

Page	Address [hex]	Bit								Initialize Value
		7	6	5	4	3	2	1	0	
7	02	Temp Max Limit Offset [7:0]								8'h00
	03	Temp Offset [7:0]								8'h00
	04	Temperature Limit[7:0]								8'h7D
	05	Temperature output[7:0]								N/A

Table 20 **Temperature Alarm Limit setting and Temperature Output Address**

Table 21 shows examples based on an initial Alarm (0x04) setting of 125 °C. The temperature offset can be a positive or negative value.

	Temperature Sensor Offset Register	0x02	0x03	0x04	0x05	
Case	**Offset Value (Decimal)**	**Temperature Upper Limit Offset (hex)**	**Temperature Offset (hex)**	**Temperature Upper Limit (hex)**	**Temp Output Data (Dec)**	**Alarm Trigger**
1	0	0	0	7D	124	N
					125	Y
					126	Y
2	10	0A	0A	7D	124	N
					125	Y
					126	Y
3	-1	0	FF	7D+01	124	N
					125	Y
					126	Y
4	-10	0	F6	7D+0A	124	N
					125	Y
					126	Y

Table 21 **Temperature Sensor Offset Setting Example**

NOTE

1. Case 1: No offset scenario.
2. Case 2: If the temperature offset (0x03) is positive value, then the Temp. Upper Limit Offset (0x02) is also set to the same value.
3. Case 3: If the temperature offset (0x03) is negative value, then the absolute value of this value needs to be added to the default Temp. Upper Limit (0x04).
4. Case 4: Another negative offset value example.

5 Calibration of the N20MA-M42M Encoder

5.1 Full Auto-Calibration with Accuracy Correction Enabled

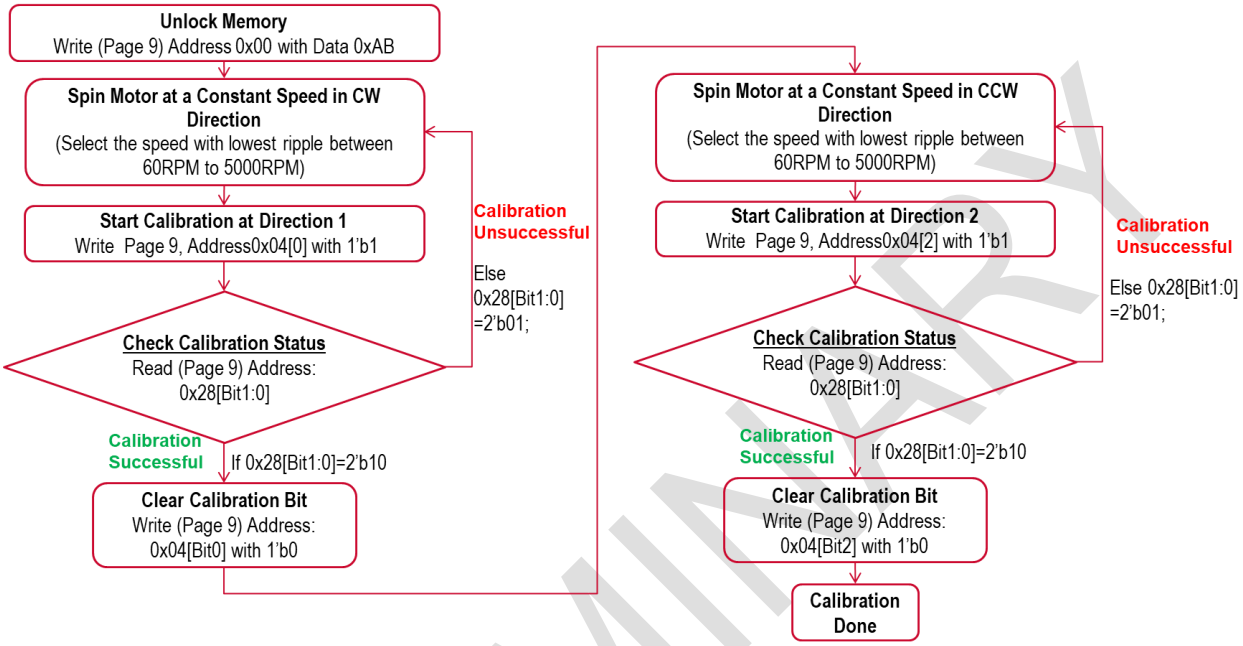

Figure 5 Flow chart for full auto-calibration process

5.1.1 Calibrate in Clockwise (CW) Direction

1. Unlock Memory (Write Page 9, Address 0x00 = 0xAB)
2. Spin the spindle motor at CW direction at 60RPM to 5000rpm (recommend to select the least ripple speed, not to exceed 5000RPM). Wait for the motor speed to be stable before start the next step.
3. Write Page 9, Address 0x04[0] = 1b
4. Loop Reading Calibration Status Address 0x28
5. If Address 0x28[1:0] = 00b Calibration in-progress; 10b Calibration Done; 01b Calibration Error
6. Clear the Calibration Register, Address 0x04 = 0h. Repeat the steps 3 to 5 above if unsuccessful, e.g. up to 10x retry

5.1.2 Calibrate in Counter-Clockwise (CCW) Direction

1. Spin the spindle motor at CCW direction at 60RPM to 5000rpm (recommend to select the least ripple speed, not to exceed 5000RPM). Wait for the motor speed to be stable before start the next step.
2. Write Page 9, Address 0x04[2] = 1b
3. Loop Reading Calibration Status Address 0x28
4. If Address 0x28[1:0] = 00b Calibration in-progress; 10b Calibration Done; 01b Calibration Error
5. Clear the Calibration Register, Address 0x04 = 0h. Repeat the steps 2 to 4 above if unsuccessful, e.g. up to 10x retry

5.2 Auto-Calibration without Accuracy Correction

1. Unlock Memory (Write Page 9, Address 0x00 = 0xAB)
2. Spin the spindle motor at CW direction at 60RPM to 5000rpm (recommend to select the least ripple speed, not to exceed 5000RPM). Wait for the motor speed to be stable before start the next step.
3. Write Page 9, Address 0x04[1] = 1b
4. Loop Reading Calibration Status Address 0x28
5. If Address 0x28[1:0] = 00b Calibration in-progress; 10b Calibration Done; 01b Calibration Error
6. Clear the Calibration Register, Address 0x04 = 00h. Repeat the steps 3 to 5 above if unsuccessful, e.g. up to 10x retry.

5.3 Auto Zero-Reset (Single-Turn)

1. Unlock Memory
2. Write Page 9, Address 0x02[1] = 1b
3. Program Memory (Write Page 9, Address 0x01 = 0xC0)

5.4 Auto Zero-Reset (Multi-Turn)

1. Unlock Memory
2. Write to Page 9, Address 0x02[0] = 1b
3. Program Memory (Write Page 9, Address 0x01 = 0xC0)

5.5 Alarm Clear

1. Unlock Memory
2. Write to Page 9, Address 0x02[2] = 1b

5.6 EH Pulse Voltage Monitoring

The N20MA has a built-in function to measure and monitor the EH pulse voltage level (VWC). Measurement must be conducted with the final encoder assembly inclusive of the external cover.

1. Unlock Memory (Write Page 9, Address 0x00 = 0xAB)
2. Enable VWC Monitoring Self Check by writing Address 0x08 = 04h
3. Spin the spindle motor at CW direction for > 350 rotations at 3000rpm
4. Loop Reading Calibration Status Page 9, Address 0x45
5. If Address 0x45[3] = 1b Measurement Done
6. End VWC Monitoring Self Check by writing Page 9, Address 0x08 = 00h
7. Read Page 9, Address 0x46 to 0x47 for the measured data.
8. Stop the Motor. Repeat step 2-7 with CCW direction.

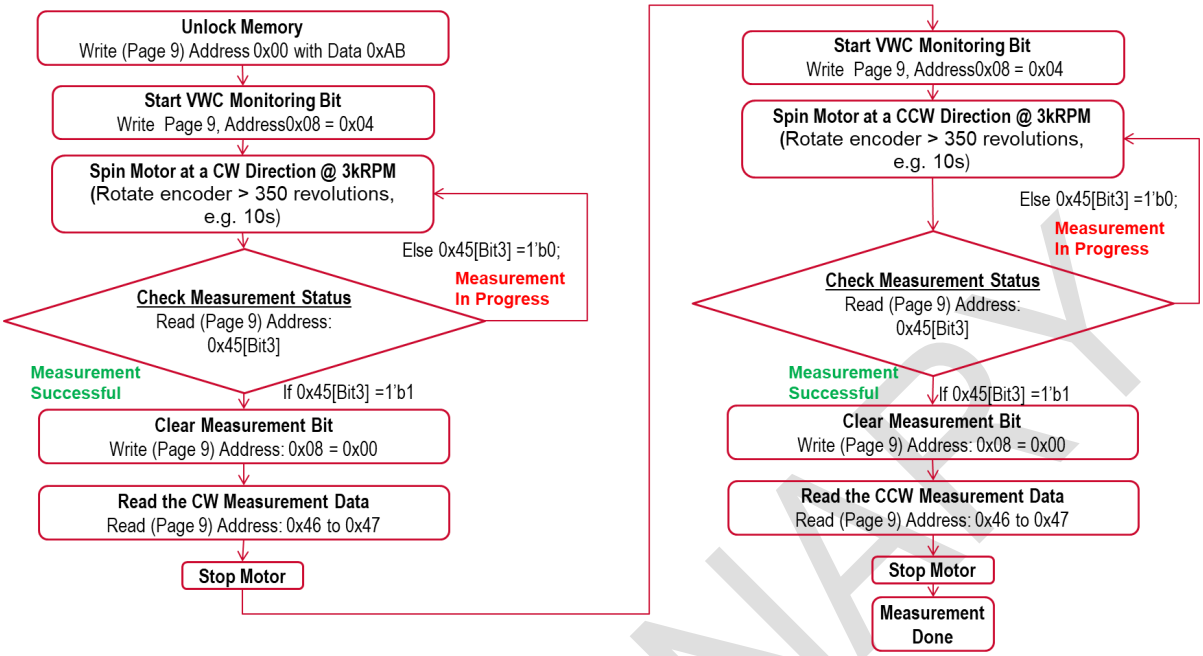

Figure 6 VWC Monitoring Self Test Flow Chart

Page	Byte Address		Description	Bit							
Page [dec]	[dec]	[hex]		7	6	5	4	3	2	1	0
9	8	08	Command						Vwc_Mon_Trig		
	69	45	Status					VWC Result Ready			
	70	46	MT Counter VWC	EH Pulse VWC data, Average – 4 Sigma (Target value: 48 to 80 decimal)							
	71	47		EH Pulse VWC data – Mean (Target 48 to 80 decimal)							

Table 22 **EH Pulse Monitoring Measurement Registers**

5.7 Code Monotony Measurement

The N20MA has a built-in function to measure and monitor the code monotony of the ST position data. Measurement must be conducted with the final encoder assembly inclusive of the external cover.

1. Unlock Memory (Write Page 9, Address 0x00 = 0xAB)
2. Enable Code Monotony measurement by writing Page 9, Address 0x06 = 01h
3. Spin the spindle motor at CW direction for > 3 revolutions at low speed, e.g. 2RPM to 10RPM
4. Read Page 9, Address 0x60 to 0x63 for the measured data.
5. End the Code Monotony measurement by writing Page 9, Address 0x06 = 00h
6. Stop the Motor. Repeat step 2-5 with CCW direction.

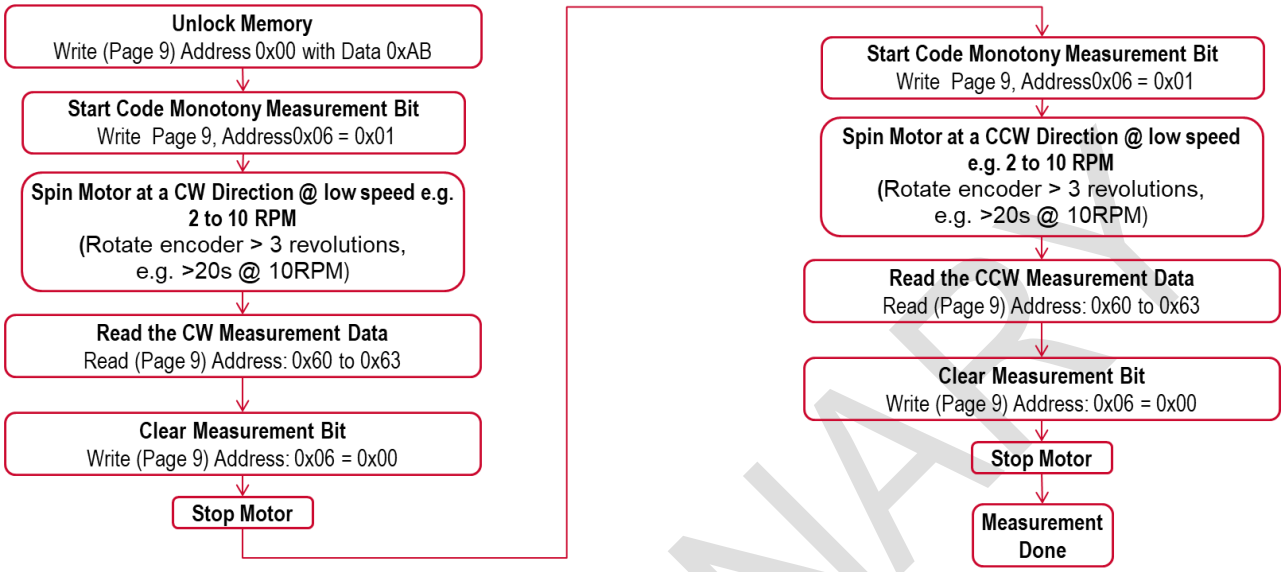

Figure 7 Code Monotony Self Test Flow Chart

SPI	Byte Address		Description	Bit							
Page [dec]	[dec]	[hex]		7	6	5	4	3	2	1	0
9	6	06	CM Test								CM_Test_En
	96	60	CM_Max[15:0]	CM_Max[15:0]							
	97	61									
	98	62	CM_Min[15:0]	CM_Min[15:0]							
	99	63									

Table 23 **Code Monotony Measurement Registers**

We are here for you. Addresses and Contacts.

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